

VLSI Implementation of a Neuromime Pulse Generator for Eckhorn Neurons

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The Eckhorn neuron model has important applications in image processing by means of pulse-coded neural networks. It is composed of two principal parts, the dendrite and the neuromime pulse generator. This paper discusses a VLSI design of a neuromime pulse generator for implementation in Eckhorn neurons.

Introduction: The Eckhorn neuron model (ENM) is presently the most commonly used neuron in artificial pulse-coded neural network (PCNN) implementations in the field of image processing. The ENM was proposed in 1990 by Eckhorn et al. [1] as a means to achieve feature-linking and region-linking among distributed assemblies of neural sub-networks. Although it is not the only artificial neuron capable of producing synchronized firing patterns from assemblies of neurons [2], its simplicity relative to previous non-integrate-and-fire pulse coded neuron models and the flexibility of its structure have both contributed to its popularity in engineering applications. The ENM has demonstrated not only the ability to achieve time-locked, synchronous firing patterns in PCNN's, but has also been shown to produce networks with such desirable features as insensitivity to input field translations, rotations, and scaling [3]. These are the features that the integrate-and-fire neuron (IFN) has not convincingly demonstrated to date.

In most artificial neural network (ANN) implementations, the basic neuron element is a single-compartment model, which means the neuron models the entire

neuron cell. In contrast, the ENM is a multi-compartment neuron model. A simplified representation of the ENM is depicted in Fig. 1. The ENM separates the functions of the cell body (soma) and dendrite, and a single neuron may have multiple dendrites. The ENM dendrites carry out most of the signal processing performed by the neuron and the soma is used as an output pulse generator. The key feature of the ENM is the linking field structure, and it is the linking field that is responsible for the ability of the ENM to achieve time-locked synchronous firing patterns in cell assemblies. The remainder of this paper focuses solely on the VLSI implementation of the neuromime pulse generator (NMPG), which converts the net dendritic activity, U_m , into a pulsed output.

Circuit: A schematic of the NMPG circuit is shown in Fig. 2. The circuit receives an input signal representing the total dendrite activity, U_m , and generates a pulsed output at a frequency approximately proportional to the magnitude of the input signal.

The critical functions of the NMPG are a comparator and a feedback leaky integrator (LI), which was previously reported in [4]. The comparator is implemented with transistors M1-M4 while the LI is comprised of transistors M10-M17. The non-inverting input to the comparator is the gate of M3, which is a magnitude signal representing the net activity, U_m , from a dendrite. The output of the comparator is at the drain of M4, which controls a switch comprised of transistors M7 and M8. Increasing U_m increases the drain current of M3, and if this current exceeds the drain current of M4 the comparator output goes HIGH. The inverting input of the comparator (gate of M4) receives the LI output (drain of M16), and if the drain current of M4 exceeds that of M3 the comparator output will go LOW.

A LOW comparator output shunts current source I_{pg} to ground through switch transistor M7 leaving the LI operating under nominal bias conditions set by current source I_{bias} . A HIGH comparator output shunts I_{pg} through switch transistor M8 to a summing resistor (SR) implemented by transistor M9 operating in the triode region. The additional current drawn through M9 while the comparator output is HIGH results in the activation of the LI. The LI signal is fed back to the inverting input to the comparator comprised of a differential amplifier implemented by transistors M4, M5, and M6 with M6 operating in the triode region as a resistor. The function of M6 is to provide source degeneration for transistor M3. Correspondingly, as the LI output increases, the current through M6 increases and the result is a decrease in the drain current of M3 allowing the comparator output to reset. Table 1 lists the W/L ratios of the transistors.

Results: Fig. 3 shows the output of the NMPG in response to an increasing input signal, U_m . The input signal starts at 0 volts and is initially stepped up to a value of 1.5 volts (the threshold at which the pulse generator begins generating symmetric pulses). The magnitude of the input signal is then increased in increments of 0.1 volts for the remainder of the simulation. Notice that the increasing input signal level gives rise to an increase in the firing rate of the pulse generator.

Fig. 4 depicts the frequency vs. input voltage level of the NMPG circuit for voltages ranging from 1.6 to 2.8 volts. The output frequency starts at roughly 2.2 MHz for an input voltage of 1.6 volts and increases linearly to a value of 10 MHz for an input voltage of 2.55 volts. This results in a frequency gain of approximately 9.25 MHz/volt

with an input voltage range corresponding to 20% of the supply voltage (+5V for this design).

Conclusion: This paper has presented an economical VLSI implementation of a neuromime pulse generator for use in Eckhorn neurons, which have demonstrated the ability to achieve time-locked, synchronous firing patterns in PCNN's. The circuit makes use of a comparator circuit in conjunction with a single leaky integrator to produce a pulsed output at a frequency proportional to the magnitude of the input signal. The design produces all neuromime properties required by the Eckhorn scheme including a minimum firing threshold level and single-time-constant ac thresholding following the generation of an action potential. Prototypes of the pulse generator have been fabricated by MOSIS™ using a 1.5μ process and are presently being tested.

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References

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Figure Captions:

Fig. 1 Simplified Eckhorn neuron model. The neuron has two types of synapses. Feeding field synapses are data-path synapses carrying the information to be processed by the network. Linking field synapses are modulatory synapses that control the type of signal processing carried out by the neuron. The net dendrite activity, U_m , is applied to the NMPG to produce a frequency-modulated output.

Fig. 2 Circuit diagram of the NMPG.

Fig. 3 Increasing pulse repetition rate for the NMPG. An increasing input signal U_m (.....) results in an increase in the pulse frequency of NMPG_out (____).

Fig. 4 NMPG output frequency vs. input voltage.

Table Captions:

Table 1: W/L ratios for CMOS transistors ($\mu\text{m}/\mu\text{m}$).

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Fig. 1

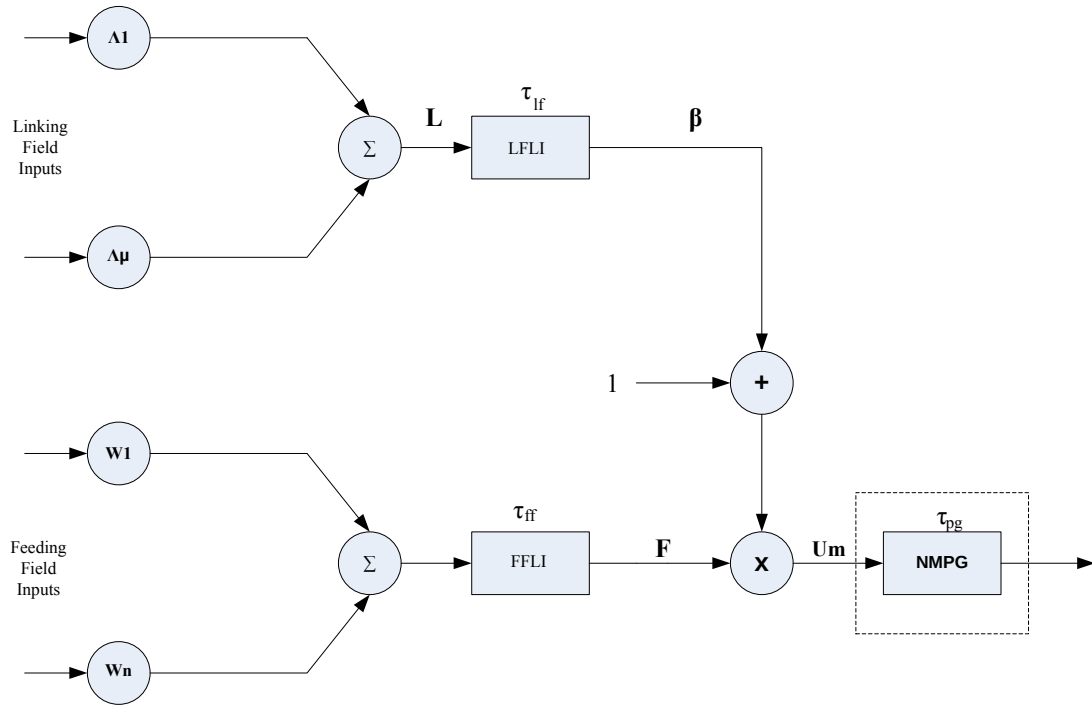


Fig. 2

Neuromime Pulse Generator

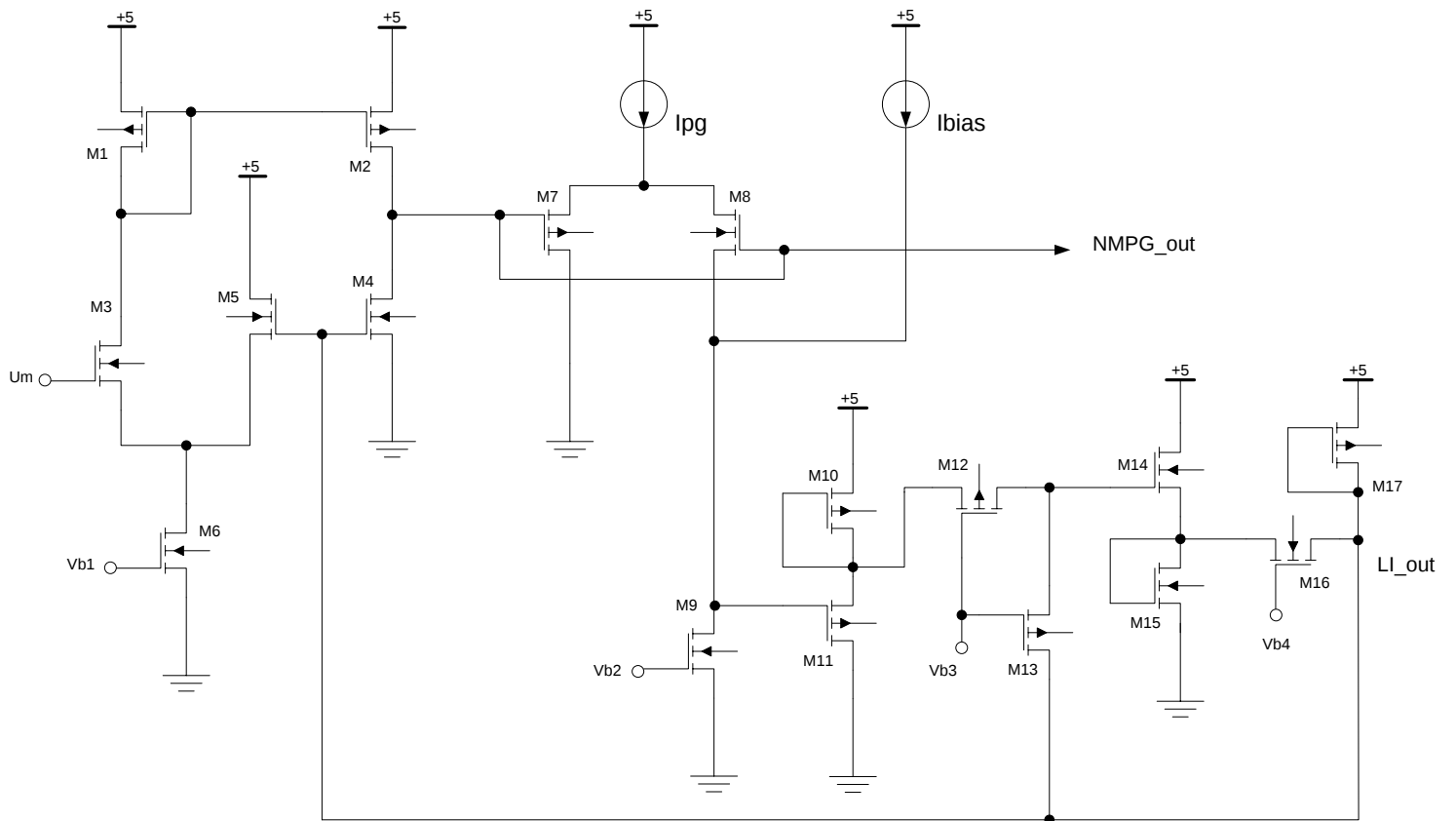


Fig. 3

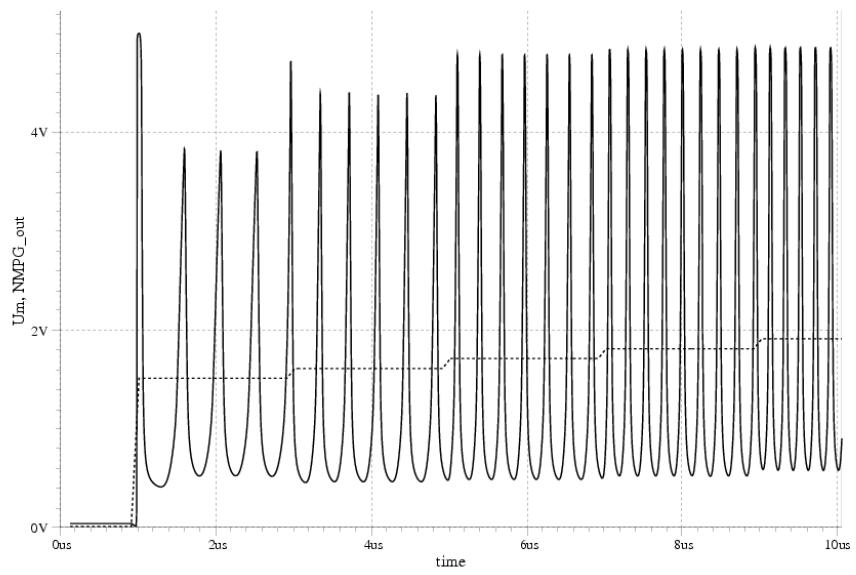


Fig. 4

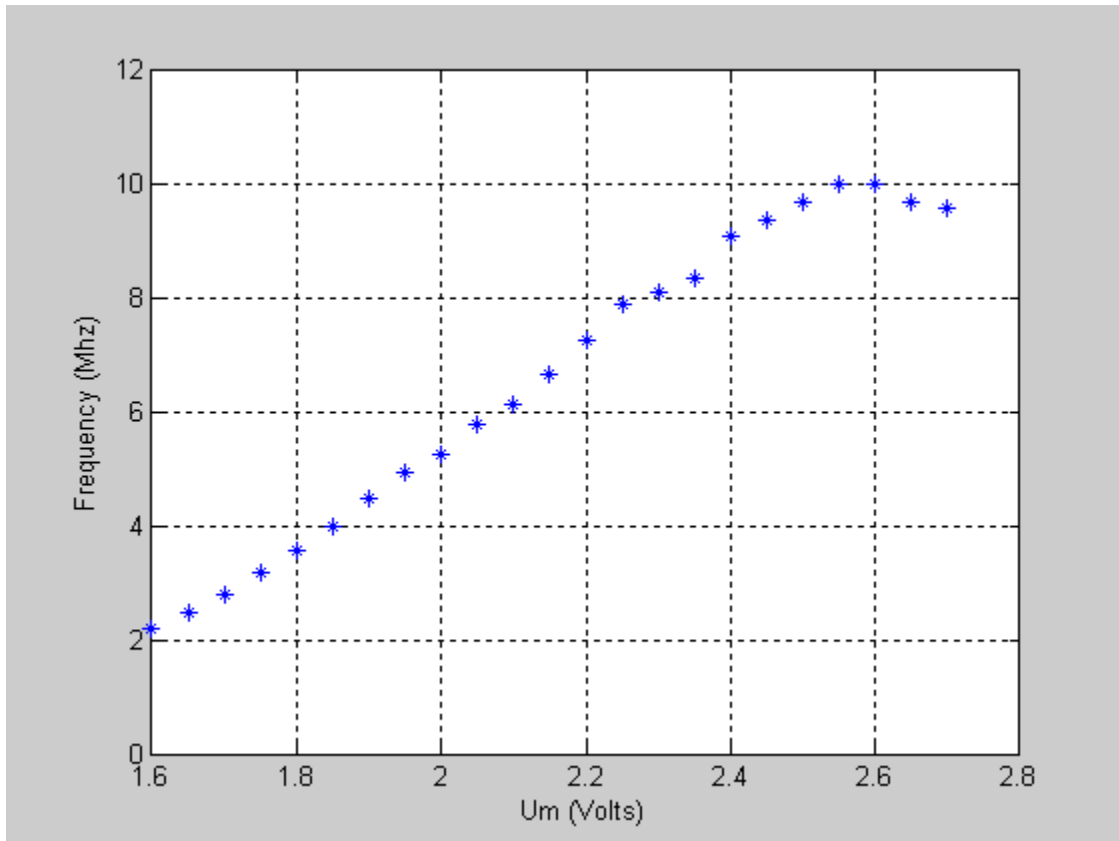


Table 1

M1	4/2	M10	4/4
M2	20/2	M11	4/4
M3	20/2	M12	4/4
M4	4/20	M13	4/20
M5	12/2	M14	8/2
M6	5/4	M15	20/2
M7	4/2	M16	20/2
M8	4/2	M17	4/15
M9	5/2		